tensilica

The Engine of SOC Design

Green Computing:

What Does it Mean for Embedded Silicon Systems?

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Electronics Inefficiency is a Global Problem

Direct energy use for all Information Technology (PCs, telephony, consumer electronics, corporate)

- 6% of all electricity
- 200,000,000,000,000 watt-hours per year (~30 800MW central baseload power plants) for U.S, alone
- Nearly 150 million tons of CO_2 per year
- Equivalent to 30 million cars

Lack of smart energy management in other major energy uses:

- Cars
- Lighting
- Heating

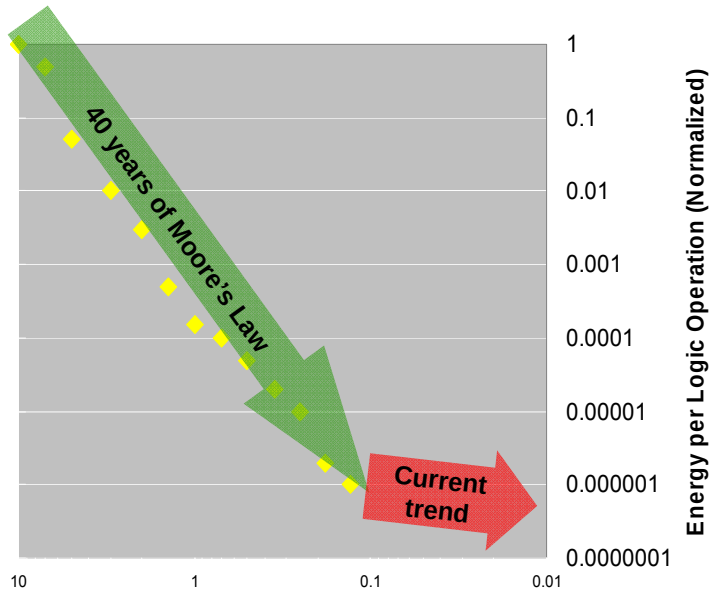
Needed:

more energy-efficient designs!

Moore's Law No Longer Helps Power
Denard Scaling Died at 90nm

The only good answer is parallel functions

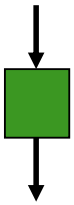
Silicon Energy Efficiency



Source: Shekhar Borkar, Intel, "Exponential Challenges, Exponential Rewards—The Future of Moore's Law", 2004

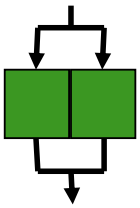
1 block:

Frequency	1
Voltage	1
Power	1
Area	1
Throughput	1



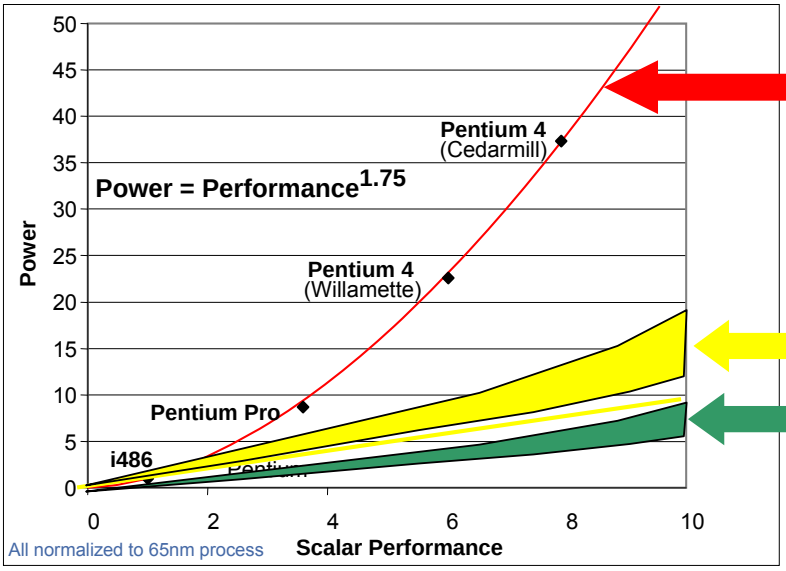
2 blocks in parallel:

Frequency	0.5
Voltage	0.5
Power	0.25
Area	2
Throughput	1



Tensilica cores have been characterized to 0.6v - ~10μW/MHz

Multi-Core Processors Lower Power



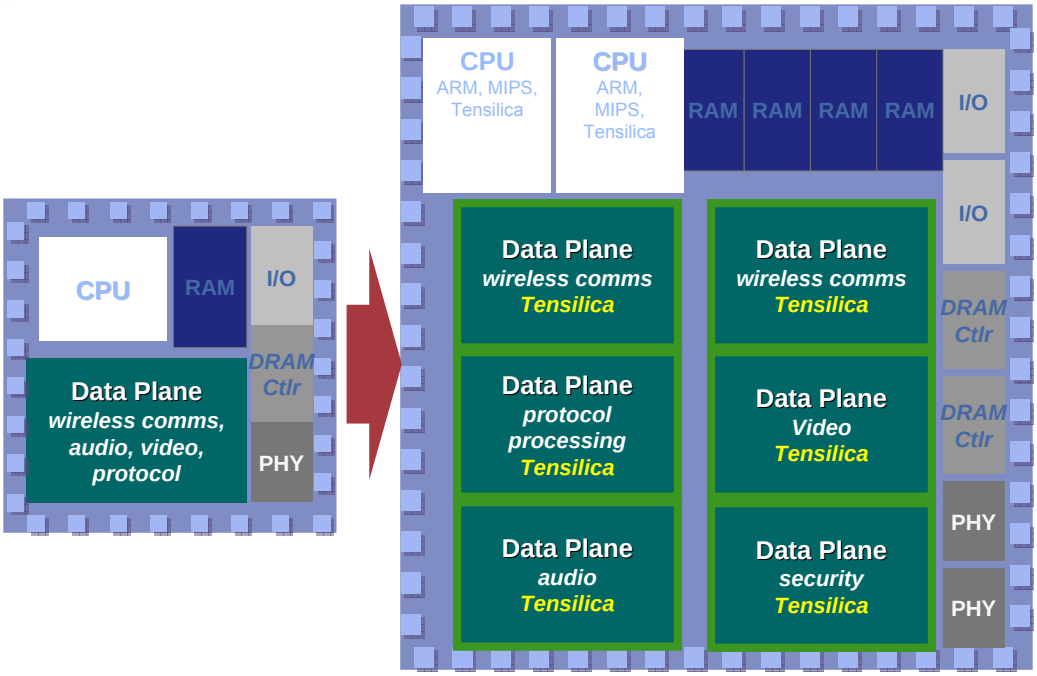
Single Core: You Need Exponentially More Power to get More Performance

Multiple Small Cores = Performance at Much Lower Power (always some efficiency loss in parallelizing software

Application-specific processor tuning further improves performance and reduces energy

Source: John Paul Shen, Intel Microarchitecture Research Lab
WCED Panel: June 18, 2006 and Tensilica

Number of Processors Increasing with Smaller Geometries



Control Plane:

- Need more performance
- General-purpose software
- Big challenge: Rewriting software for parallel execution
- Hard to use multiple cores

Data Plane:

- Need **lots** more performance
- Shift to processor-based data-plane
- Parallelism among functions makes it easy to use multiple cores
- Big challenge: Finding common architectures to ease integration

Formula for Energy Efficiency Success

Multi-core Design

- Many small cores
- Interfaces, memory and bus
- Modeling and software development

+

Optimized Processor

- Easy to configure and extend for exact application and lowest power
- Tools automatic processor creation: High differentiation, low pain:
- Proven solutions for networking, multimedia, wireless and consumer

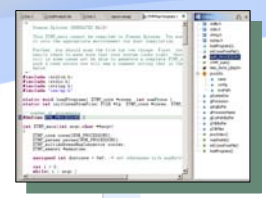
=

Energy Breakthrough

- Battery life and mobility
- Simplified packaging, power, cooling
- Reduced product and operating costs
- Lower environmental impact

Low Energy Processor Opportunity

1 optimized instruction = 5-50 RISC instructions



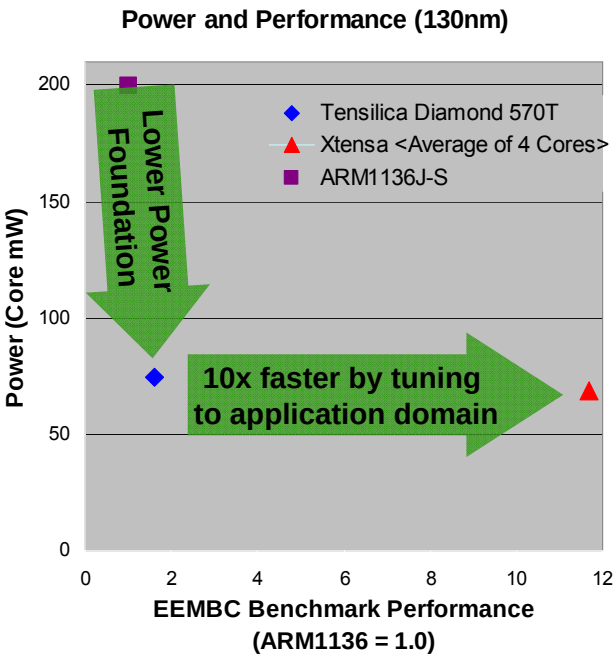
Select or describe processor configuration

Xtensa *Processor Generator*

Processor Extensions

Complete Hardware Design

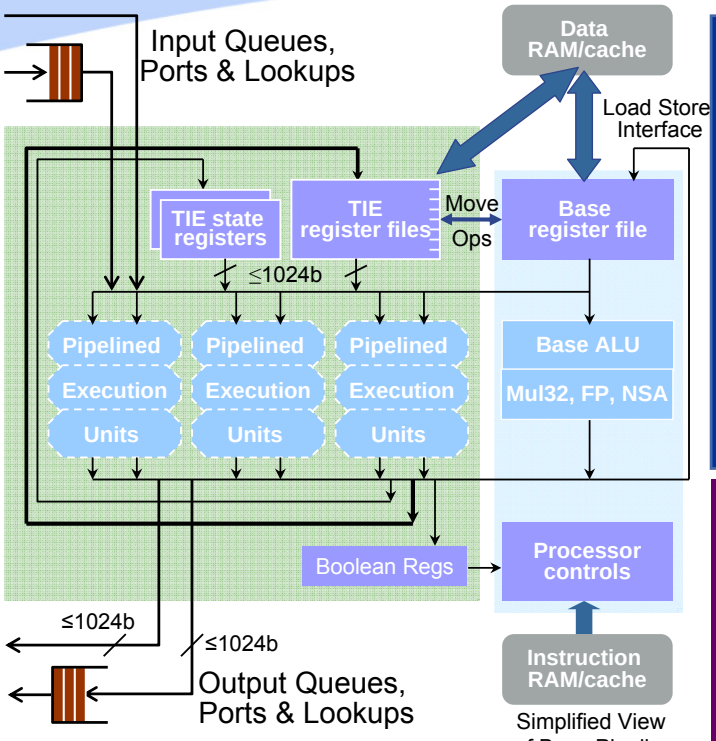
Complete Software Environment



Performance on EEMBC benchmarks aggregate for Consumer, Telecom, Office, Network, based on ARM1136J-S (Freescale i.MX31),Tensilica Diamond 570T, Xtensa LX, T1050 and T1030, All power figures from vendor websites, 2/23/2006

Key Technologies

Tensilica Instruction Extension (TIE)



Simplified View of Base Pipeline

1. **Start with base Xtensa core**
2. **Add functional units from menu of config options**
3. **Add register files and state registers**
   Add corresponding new data types with automatic C/C++ compiler support
4. **Add up to 128-bit Load/Store instructions**
5. **Add multi-cycle, SIMD arithmetic and logic function units**
   Up to 64 source, destination registers
6. **Create multi-issue VLIW datapath**

A simple TIE example – VLIW processor with 128b data types and operations

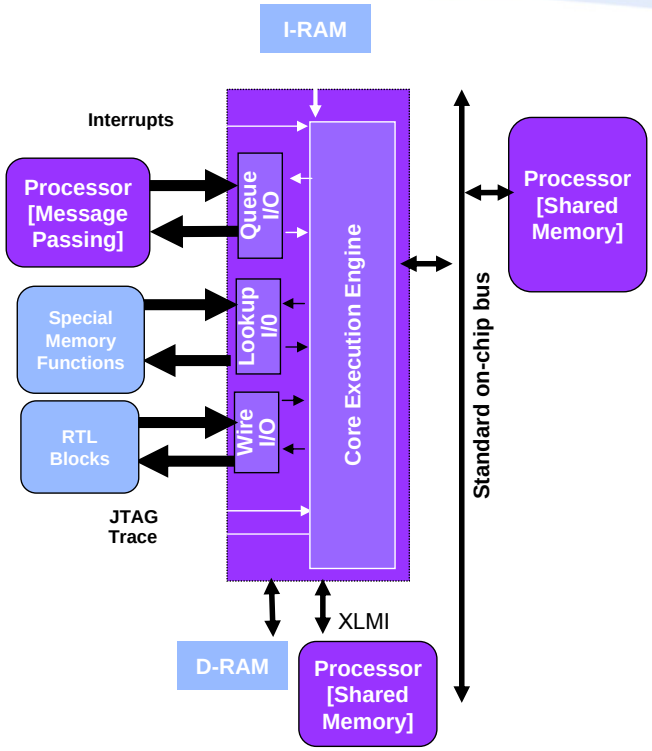
```
regfile wd 128 16 w
operation wadd {in wd a, in wd b, out wd
 c} {} {assign c = a + b;}
format f64 64 {ls_slot, alu_slot}
slot_opcodes ls_slot {LD.wd, ST.wd,L32I,
 L16UI, L16SI, L8UI, BNE, BEQ, BEQI}
slot_opcodes alu_slot {wadd, ADD, ADDI,
 SUB,SLL,SRL,SRA,SRAI,SLLI,AND,OR, EXTUI}
```

Key Technologies
New Communications Support Multi-Core

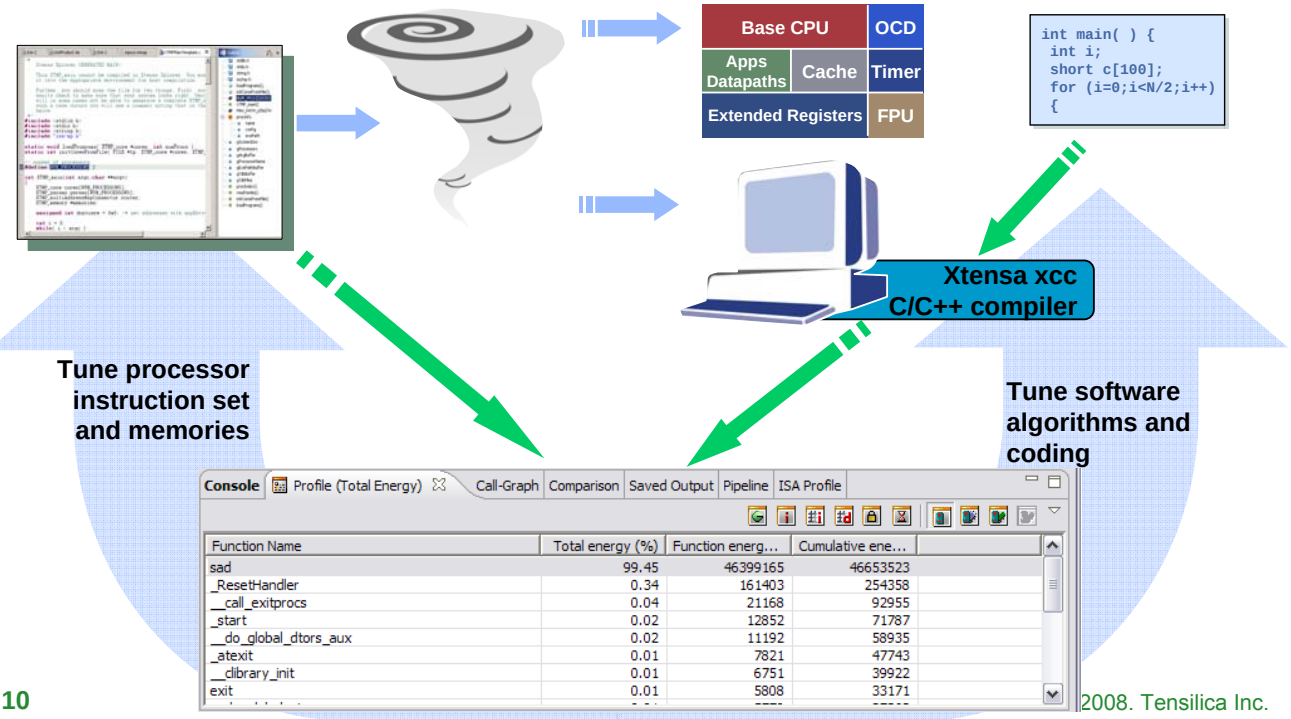
Conventional processors have limited communications potential

Xtensa creates a huge range of memory-mapped and direct connection options

- **Shared memory communication interfaces**
  - on system bus
  - in local memory
- **Message-based communication interfaces**
  - Direct connect input/output wires
  - Input and output queues
  - Lookup interfaces create any number of memory ports
- **Cuts communication overhead**
  - No load or store instructions required to directly access data
  - Synchronization is built-in



Key Technologies
Xenergy Energy Explorer



Key Technologies
XPRES Compiler: Automatic Processor Design

Great for DSPs

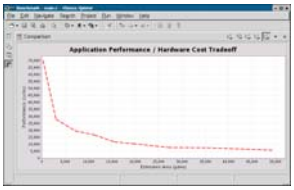
Select Reference C/C++ Code

```
short a[],b[],c[];
main() {
int i;
for (i=0;i<N;i++)
  a[i] += b[i]*c[i];
}
```

Run XPRES Compiler

Evaluates millions of possible extensions using SIMD/vector operations, operator fusion and parallel execution

Designer selects "best" configuration

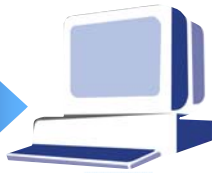


Run Xtensa Processor Generator

Complete Hardware Design

Processor

Extensions



Customized Software Tools

Compile & run unmodified C code on optimized processor

Key Technologies
Multi-Core Programming

Multi-Core Programming Models

- **Symmetric and asymmetric processor relationships**
- **Abstract Models:**
  - Shared memory
  - Message passing
  - Data-flow
  - Device driver
- **Decouple application programming model from implementation:**
  - Hardware message queues vs. memory-mapped message queues
  - Hardware vs. software cache coherency

Multi-Core Tools

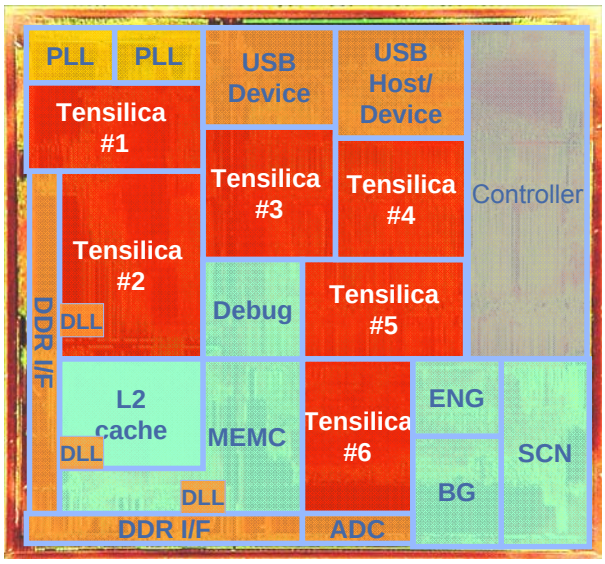
- **Rapid construction of SMP and AMP multi-core models**
  - C
  - System C
  - Coware
  - VaST
- **Direct generation FPGA prototypes for mutli-core**
- **Fully cycle-accurate MP models**
- **Fast bit-accurate "TurboXim" demonstrated to 400 CPUs in single simulation**
- **Full model + software tools support for hardware message passing**
- **Standard synchronization primitives in ISA**
- **Lightweight shared memory communications library**
- **MP OS – e.g. SMP Linux**

Multi-Core + Consumer

Most Top Printer Makers Use Tensilica

EPSON's REALOID heterogeneous, asymmetric, 6 Xtensa core design with little hard-wired logic

EPSON PM-D870



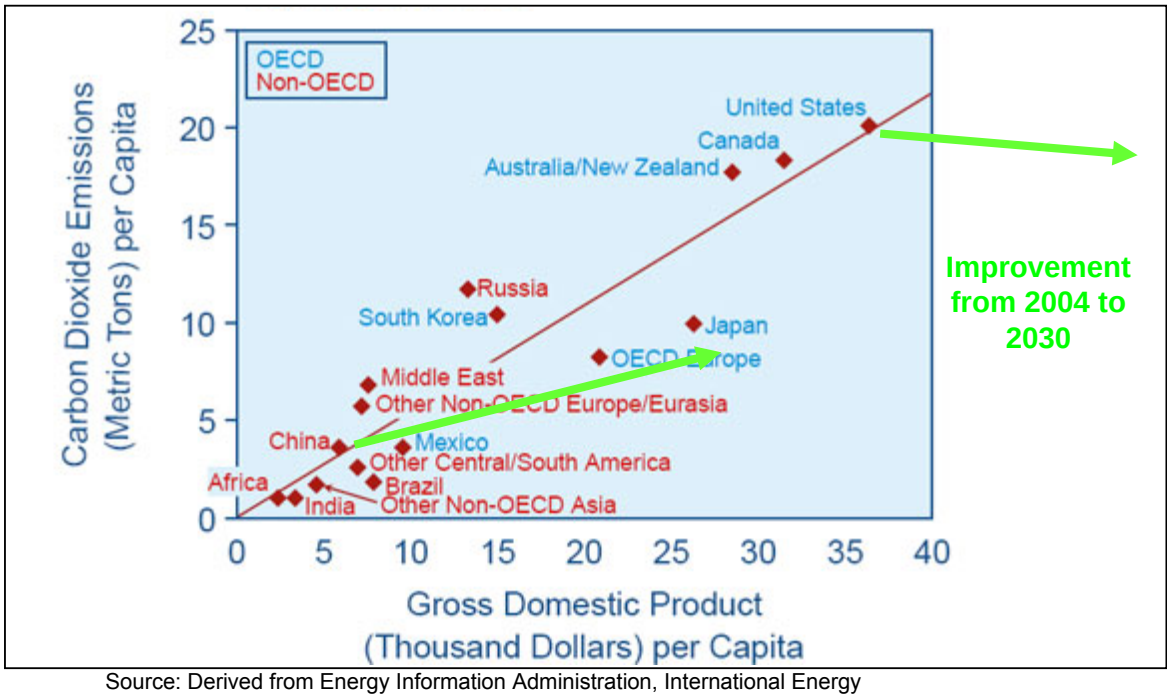
Epson REALOID IC Block Layout

90nm process technology, 100-200 MHz clock rate, 5-10M gate-count complexity, Less than 2.5W power
For more details, see the EPSON presentation, 2006 Nikkei Electronics Processor Symposium / Multi-Core Expo Japan

Multi-Core + Consumer

Mobile Feature Integration

Global Impact: Quality of Life



Source: Derived from Energy Information Administration, International Energy Annual 2004 (May-July 2006, web site www.eia.doe.gov/iea

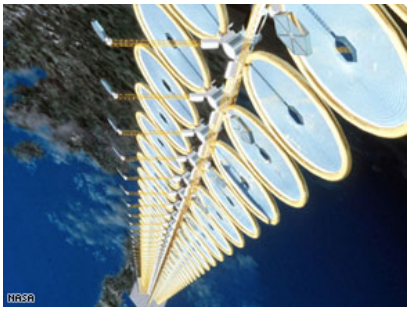
Where Now?

- **We have all the transistors—hence performance—that we need**
- **Let's teach designers to use these systems resources efficiently**

  Tuned processors with parallel execution paths running at low clock rates

  Appropriate communications running at reduced bandwidths

Last Word:
We're not running out of energy



"A single kilometer-wide band of geosynchronous Earth orbit experiences enough solar flux in one year to nearly equal the amount of energy contained within all known recoverable conventional oil reserves on Earth today."

2007 Study by the US Pentagon's National Security Space Office